IN THE CLAIMS:

1. (Currently Amended) A phase-locked loop (PLL), comprising:

a digital feedback delay line having a plurality of taps with each of said taps having a fixed delay; and

tap selection logic, coupled to said digital feedback delay line, for activating one of said plurality of taps and thereby insert a corresponding delay into said PLL.

2. (Original) The PLL as recited in Claim 1 wherein each of said taps comprises a multiplexer.

3. (Original) The PLL as recited in Claim 2 wherein said multiplexer is a 2:1 input multiplexer.

4. (Original) The PLL as recited in Claim 1 wherein said digital feedback delay line has at least four of said taps.

5. (Original) The PLL as recited in Claim 4 wherein said digital feedback delay line has 32 of said taps.

6. (Currently Amended) The PLL as recited in Claim 1 wherein said plurality of taps are cascaded from an input to an output and said corresponding delay results from fixed delays associated with said activated one of said plurality of taps and subsequent ones of said plurality of taps between said activated one and said output ~~said PLL drives a latch~~.

7. (Original) The PLL as recited in Claim 1 wherein said tap selection logic comprises a register.

8. (Currently Amended) A method of programmably adjusting a phase of a reference clock signal, comprising:

passing said reference clock signal through a phase-locked loop (PLL) that includes a digital feedback delay line having a plurality of taps with each of said taps having a fixed delay; and

activating one of said plurality of taps to insert a corresponding delay into said PLL.

9. (Original) The method as recited in Claim 8 wherein each of said taps comprises a multiplexer.

10. (Original) The method as recited in Claim 9 wherein said multiplexer is a 2:1 input multiplexer.

11. (Original) The method as recited in Claim 8 wherein said digital feedback delay line has at least four of said taps.

12. (Original) The method as recited in Claim 11 wherein said digital feedback delay line has 32 of said taps.

13. (Currently Amended) The method as recited in Claim 8 wherein said plurality of taps are cascaded from an input to an output and said corresponding delay results from fixed delays associated with said activated one of said plurality of taps and subsequent ones of said plurality of taps between said activated one and said output ~~further comprising employing said PLL to drive a latch~~.

14. (Currently Amended) A synchronous sequential logic circuit, comprising:

a system clock that produces a reference clock signal;

a plurality of interconnected modules that operate synchronously to communicate data therebetween, each of said plurality of interconnected modules containing a phase-locked loop (PLL) that receives said reference clock signal and includes:

a digital feedback delay line having a plurality of taps with each of said taps having a

fixed delay, and

tap selection logic, coupled to said digital feedback delay line, for activating one of said plurality of taps and thereby insert a corresponding delay into said PLL.

15. (Original) The circuit as recited in Claim 14 wherein each of said taps comprises a multiplexer.

16. (Original) The circuit as recited in Claim 15 wherein said multiplexer is a 2:1 input multiplexer.

17. (Original) The circuit as recited in Claim 14 wherein said digital feedback delay line has at least four of said taps.

18. (Original) The circuit as recited in Claim 17 wherein said digital feedback delay line has 32 of said taps.

19. (Currently Amended) The circuit as recited in Claim 14 wherein said tap selection logic activates only one of said plurality of taps ~~PLL drives a latch~~.

20. (Original) The circuit as recited in Claim 14 wherein said tap selection logic comprises a register.